

FIG. 1A

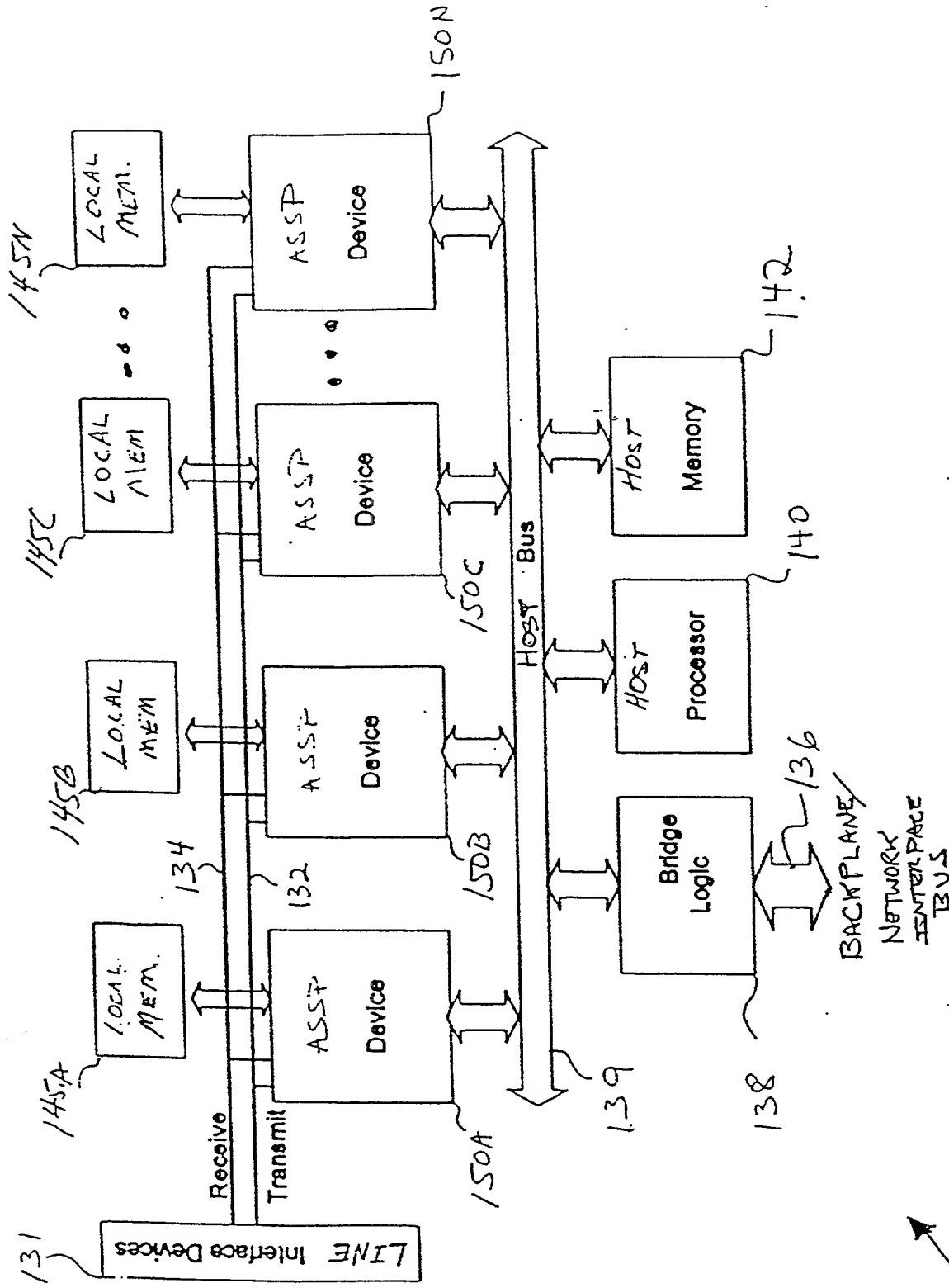


FIG. 10

130

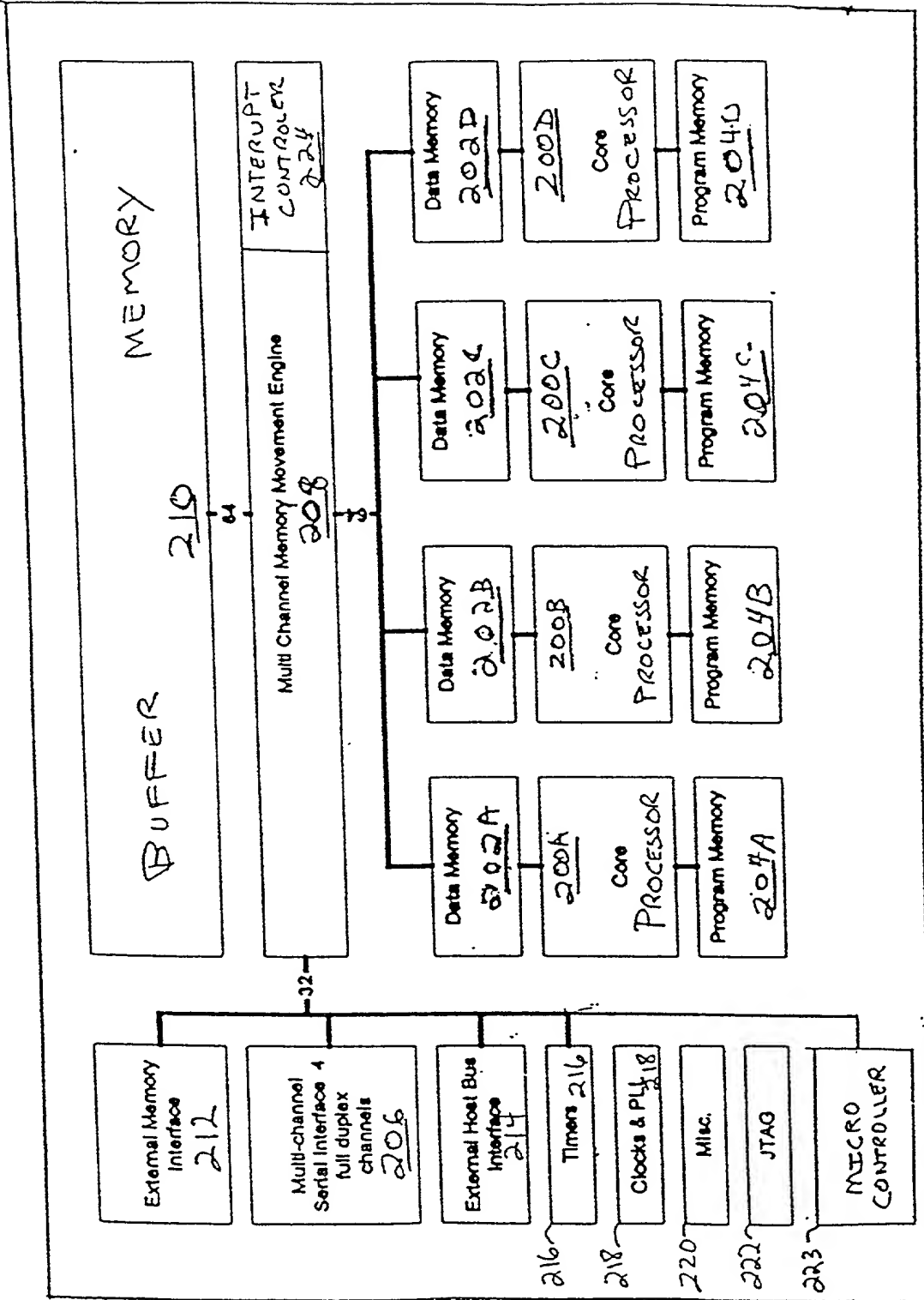


FIG. 2

FIG. 3

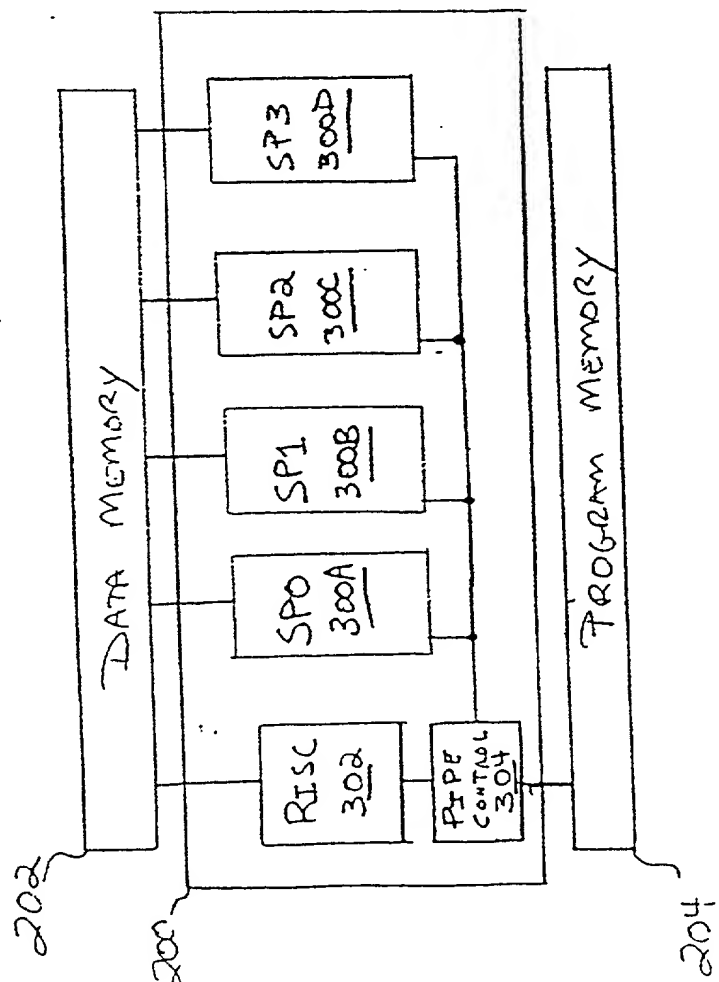


FIG. 3

FIG. 4

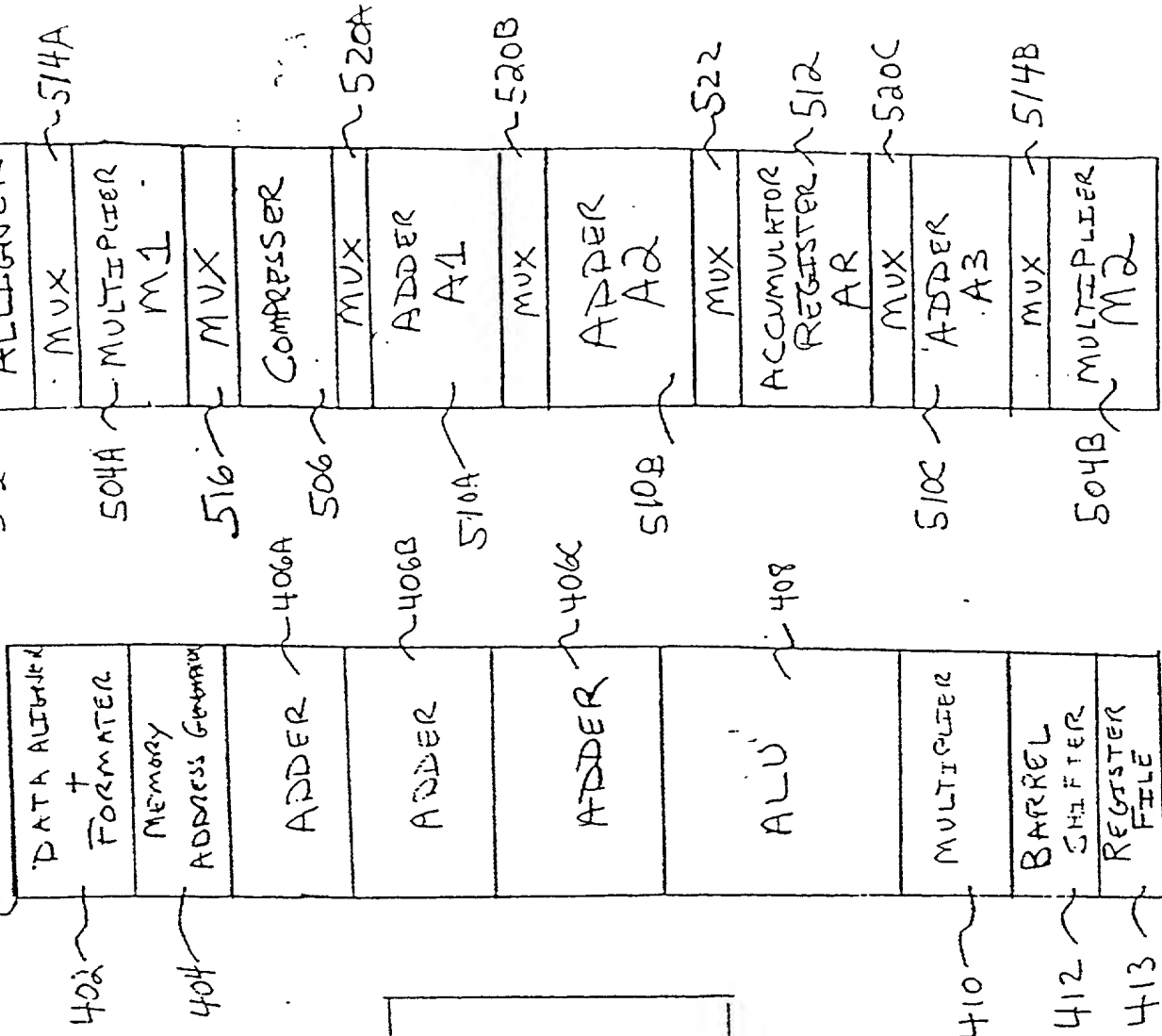
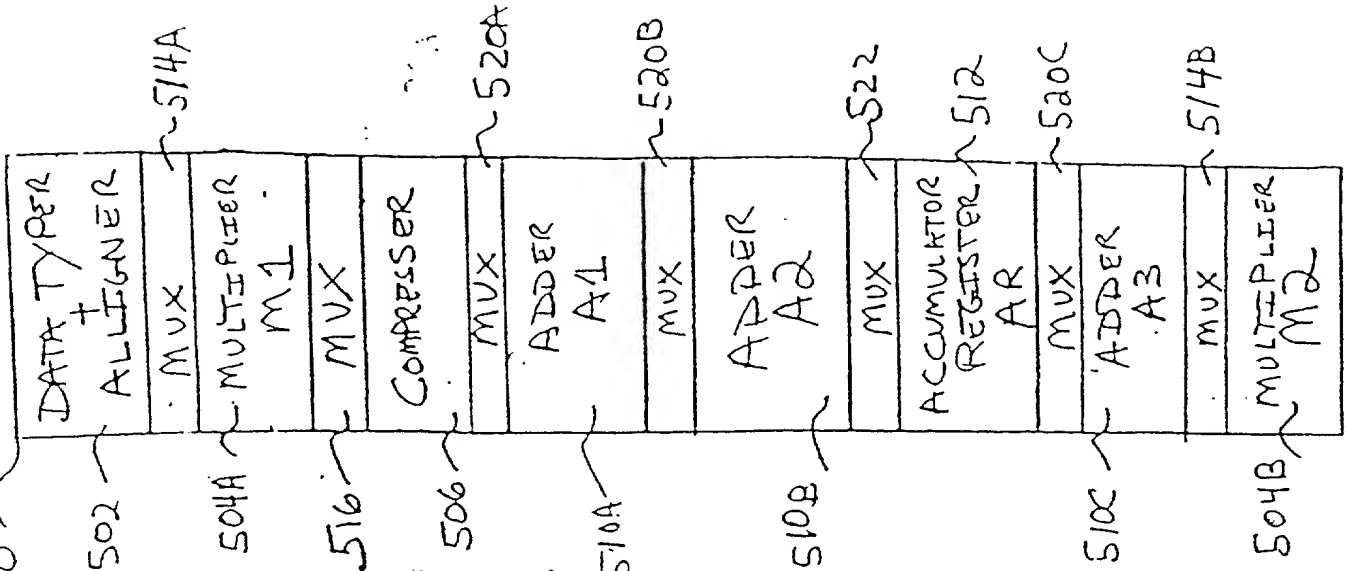


FIG. 5A



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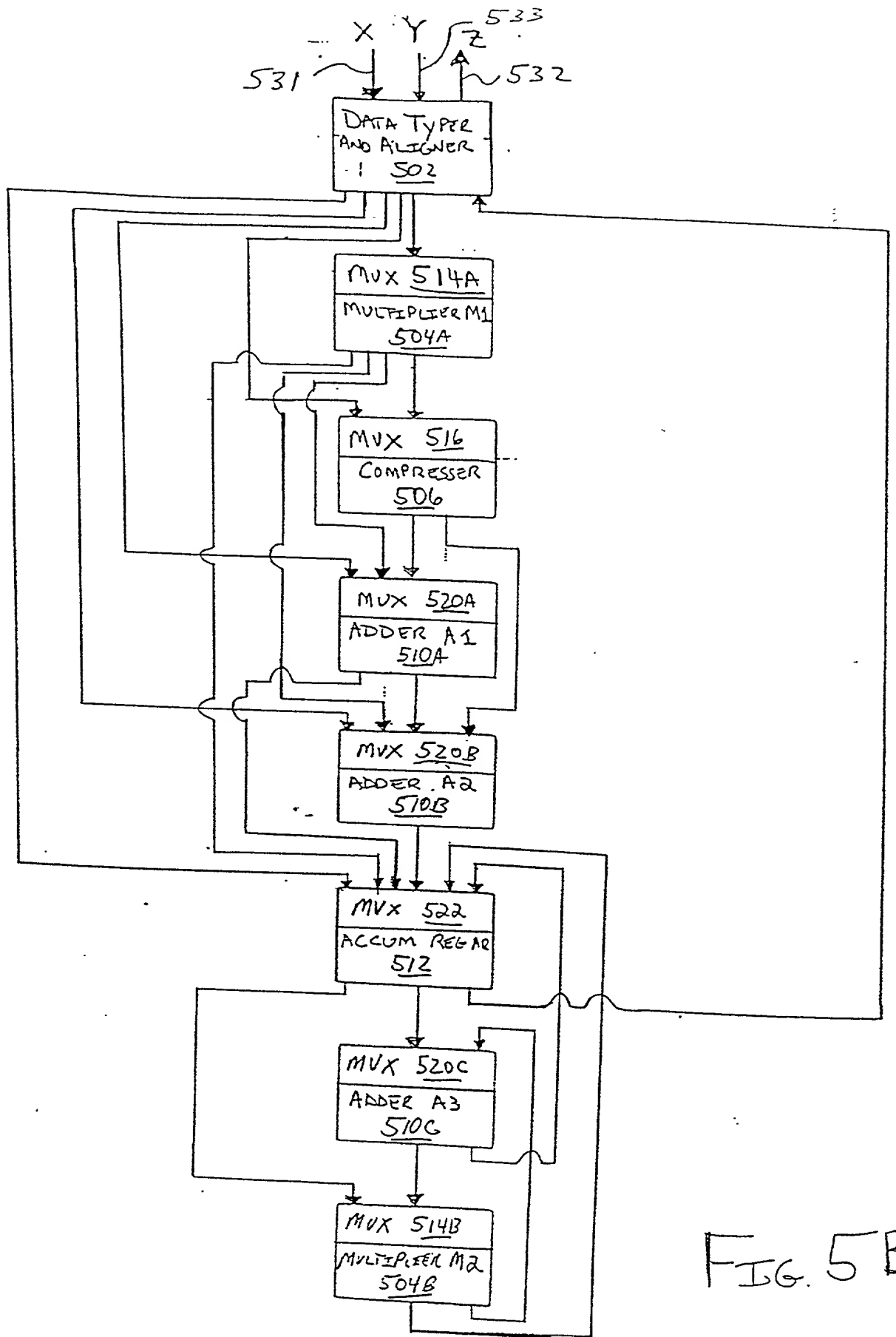
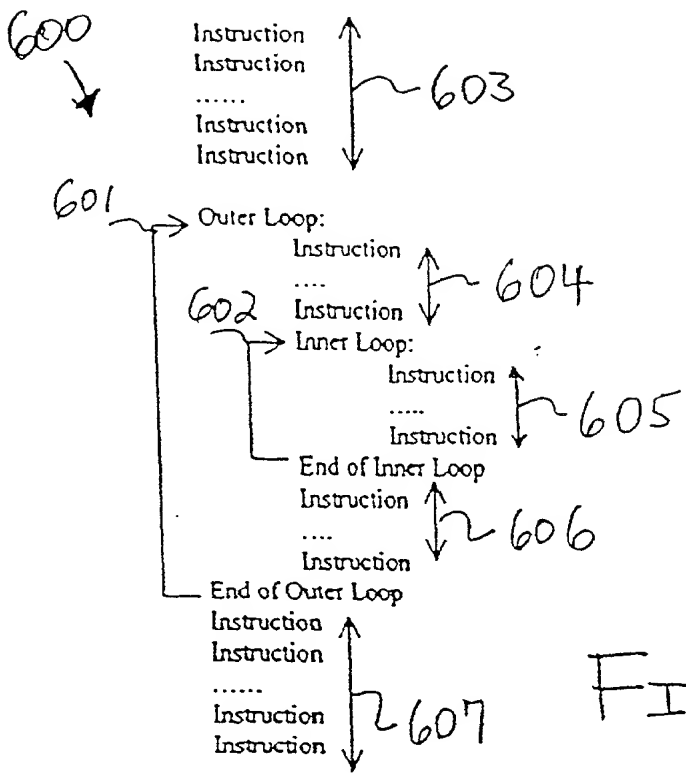


FIG. 5B



610

611 MAIN OP	612 SUB OP
MULT	NOP
ADD	MIN/MAX
MIN/MAX	ADD
NOP	MULT

FIG. 6B

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	PS	S*	SX	SY	V/S	SA	DA	Sub-op	1	Pred	PL	Sst	Syt	Rnd	S*	S*	S*	0	SA	DA	abs	0	0														
da = +/- sx*sy										Nop	0	0	0																										
da = +/- (sx*sy) + sa										Add	0	0	1											Li															
da = +/- (sx*sa) + sy										Add	0	1	0											Li															
da = +/- (sx*sy) - sa										Sub	0	1	1											Li															
da = +/- (sx*sa) - sy										Sub	1	0	0											Li															
da = max(+/- sx*sy, sa)										Min	1	0	1											Gr															
da = max(+/- sx*sa, sy)										Min	1	1	0											Gr															
da = max(+/- sx*sy, sa)										Max	1	1	1											Gr															

FIG.

FIG. 6C

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20		
1	0	0	PS	S*	SX					SY					V/S	SA	DA	0	1	0	Add
																	1	0	0	Sub	
																	1	1	0	Min	

da = +/- (mx*sa) + my
da = +/- (mx*sa) - my
da = min(+/- mx*sa, my)

FIG. 6D

20-bit ISA

39	19
0	0
0	1
1	0
1	1

Control # Control
Control # Control
DSP, extensions/Shadow
DSP # DSP

20-bit parallel
20-bit serial
40-bit extended
20-bit serial

DSP Instructions

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20
----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----

Multiply	1	0	0	PS	S*	SX	SY	V/S	SA	DA	Sub-op	
	da = sx*sy	da = (sx*sy) + sa	da = (sx*sa) + sy	da = (sx*sa) - sa	da = (sx*sy) - sa	da = (sx*sa) - sy	da = min(sx*sy,sa)	da = min(sx*sa,sy)	da = max(sx*sy,sa)	da = max(sx*sa,sy)	0	0
Add	1	0	1	PS	+/-	SX	SY	V/S	SA	DA	Sub-op	
	da = sx + sy	da = sx + sy + sa	da = sx + sy*sa = sx*sy;	da = (sx + sy) * sa	da = (sx + sy) - sa	da = min(sx*sy,sa)	da = min(sx*sy,sa)	da = max(sx*sy,sa)	da = sum(sa)	(sx, sy unused)	0	0
Extremum	1	1	0	PS	X/N	SX	SY	V/S	SA	DA	Sub-op	
	da = ext(sx,sy)	da = ext(sx,sy,sa)	da = ext(sx,sa) - sy	da = -ax(sx,sa) - sy	da = -ax(sx,sa) + sy	da = ext(sx,sa) + sy	da = ext(sx,sa) - sy	ext(sa,da) ? 1 = sx, 0 = sy, 1 = sa, 0 = lc	0	0	0	0
Type-mismatch Permute	1	1	0	PS	0	SX	SY	Type	x	x	x	1
	1	1	0	PS	1	SX	SY	Type	x	ereg	1	1
Type-mismatch Permute	1	1	1	PS	x	SX	SY	SA	DA	V/S	Sub-op	
	1	1	1	PS	x	SX	SY	SA	DA	V/S	0	0

Control and specifier Extensions

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

Mul	0	Pred	PL	Sxt	Syl	Rnd	LL	Gx	S*	S*	S*	0	SA	DA	abs	0	0	
																		Addr/Sub min/max

Add	0	Pred	PL	Sxt	Syl	Li	Sub-ext	+/-	+/-	+/-	x	V/S	Rnd	Fp	Ir-ctl	Gx	Fp	Nop (uadd) Mul/MulN Min/Max
-----	---	------	----	-----	-----	----	---------	-----	-----	-----	---	-----	-----	----	--------	----	----	-----------------------------------

Ext	0	Pred	PL	Sxt	Syl	Ir-ctl	Gx	Sub-ext	Li	Fp	Li	Fp	Sub-ext	Li	Fp	Sub-ext	Li	Addr/Sub Min/Max
-----	---	------	----	-----	-----	--------	----	---------	----	----	----	----	---------	----	----	---------	----	---------------------

0	Pred	PL	Sxt	Pc11	0	ereg	Pc11	0	0
---	------	----	-----	------	---	------	------	---	---

Type/offset/permute extensions

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

0	Pred	PL	x	Type: SX	Type: SY	0	SA	DA	x	0	1	Type override permute override Offset override
0	Pred	PL	Per	Permute: SX	Permute: SY	0	SA	DA	Per	1	0	
0	Pred	IR	Per	Offset: SX	Offset: SY	0	SA	DA	Per	1	1	

Shadow DSP

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

0	Op	PL	Op	ereg	ereg	1	SA	DA	Sub-op
---	----	----	----	------	------	---	----	----	--------

FIG. 6 E

Control instructions

Extended Control

Bits 13.2 of upper half (39.20)																			
13	12	11	10	9	8	7	6	5	4	3	2	19	18	17	16	15	14	13	12
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
UI4: length		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
UI4: outer LC		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ		RZ	
RX		RZ		RZ		RZ		RZ		RZ									

MAC:

Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1-40-bit																																								
2-20 bit																																								
2-20 bit																																								
reg																																								

MUL-HOP
MUL-ADD
MUL-EXT
MUL-MUL

ARITH:

Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																																								
1																																								
Ext																																								
Mac																																								

EXT:

Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																																								
1																																								
Ext																																								
Mac																																								

LOGIC:

Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																																								
1																																								
Ext																																								
Mac																																								

SHIFT:

Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																																								
1																																								
Ext																																								
Mac																																								

Immediate:

Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																																								
1																																								
Ext																																								
Mac																																								

Test:

Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																																								
1																																								
Ext																																								
Mac																																								

Branch:

Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0																																								
1																																								
Ext																																								
Mac																																								

Misc:

FIG. 6H

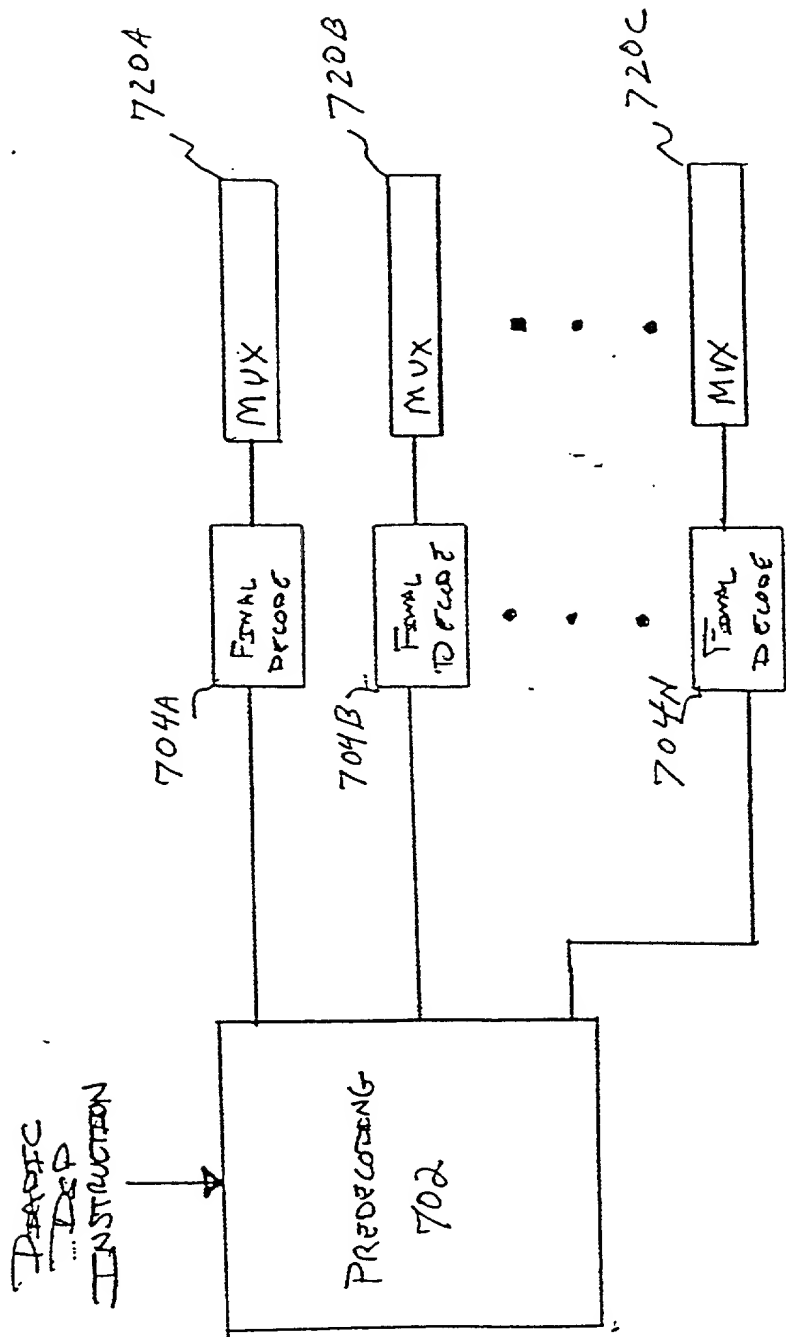


FIG. 7

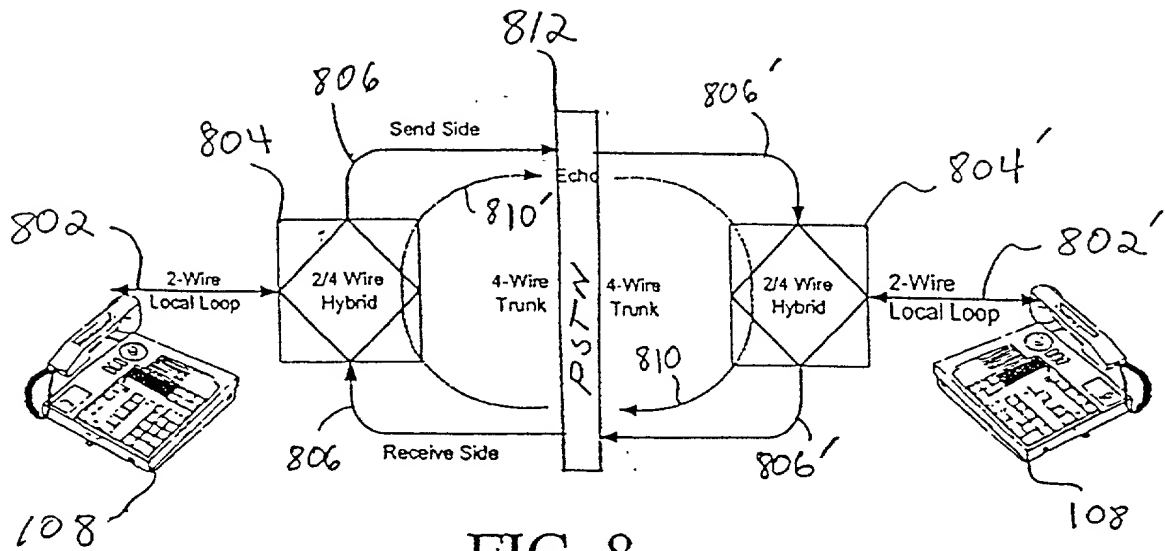


FIG. 8
(PRIOR ART)

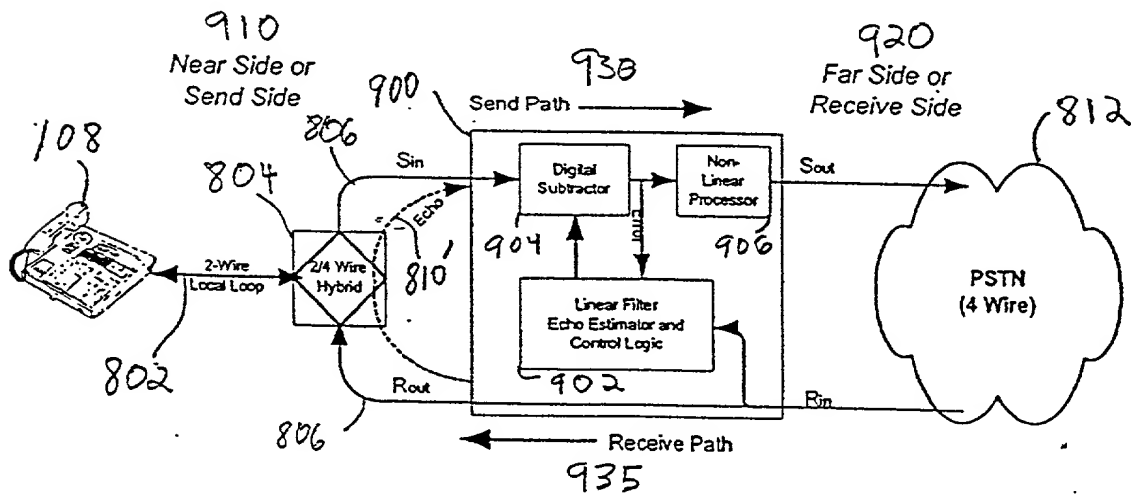
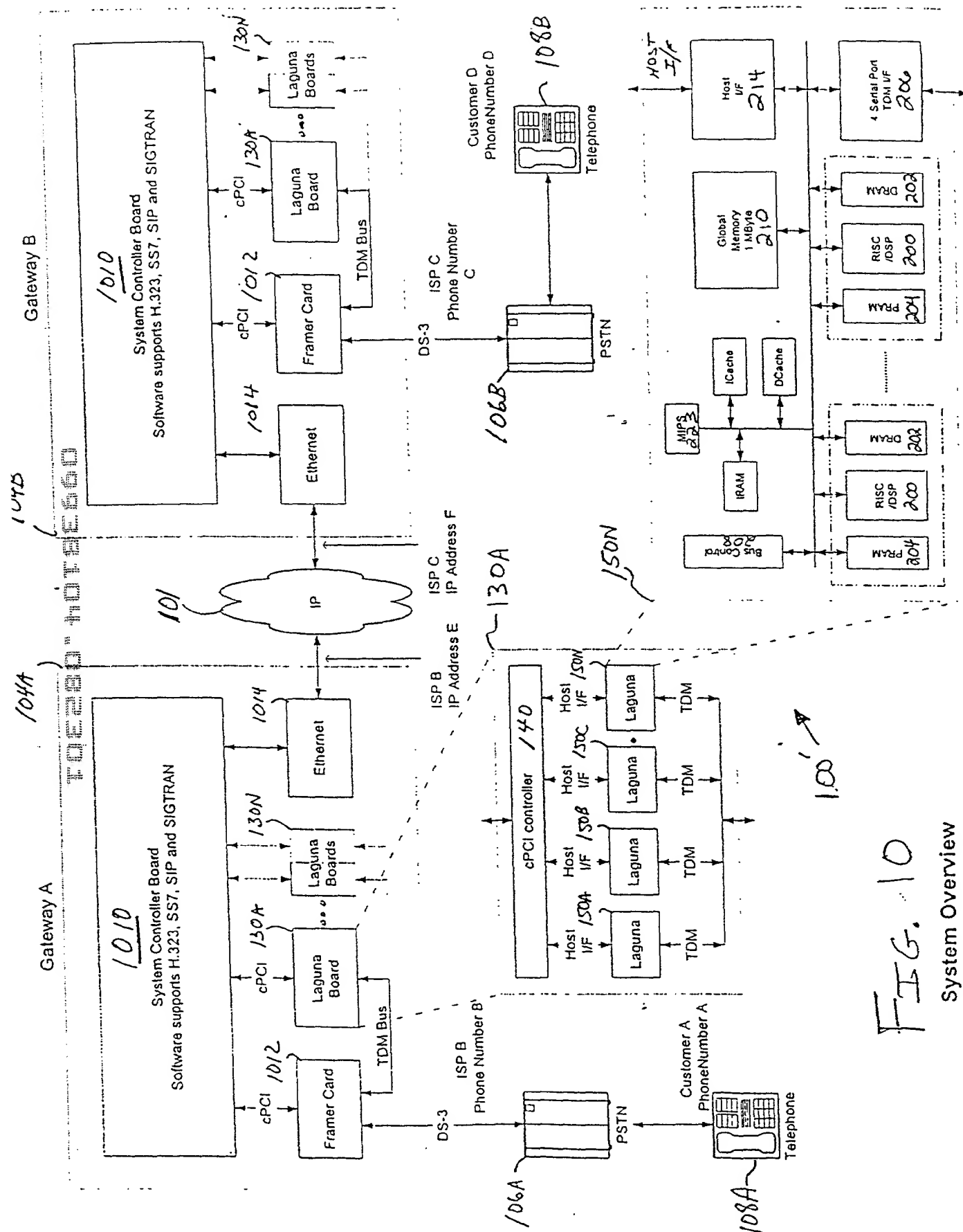


FIG. 9
(PRIOR ART)



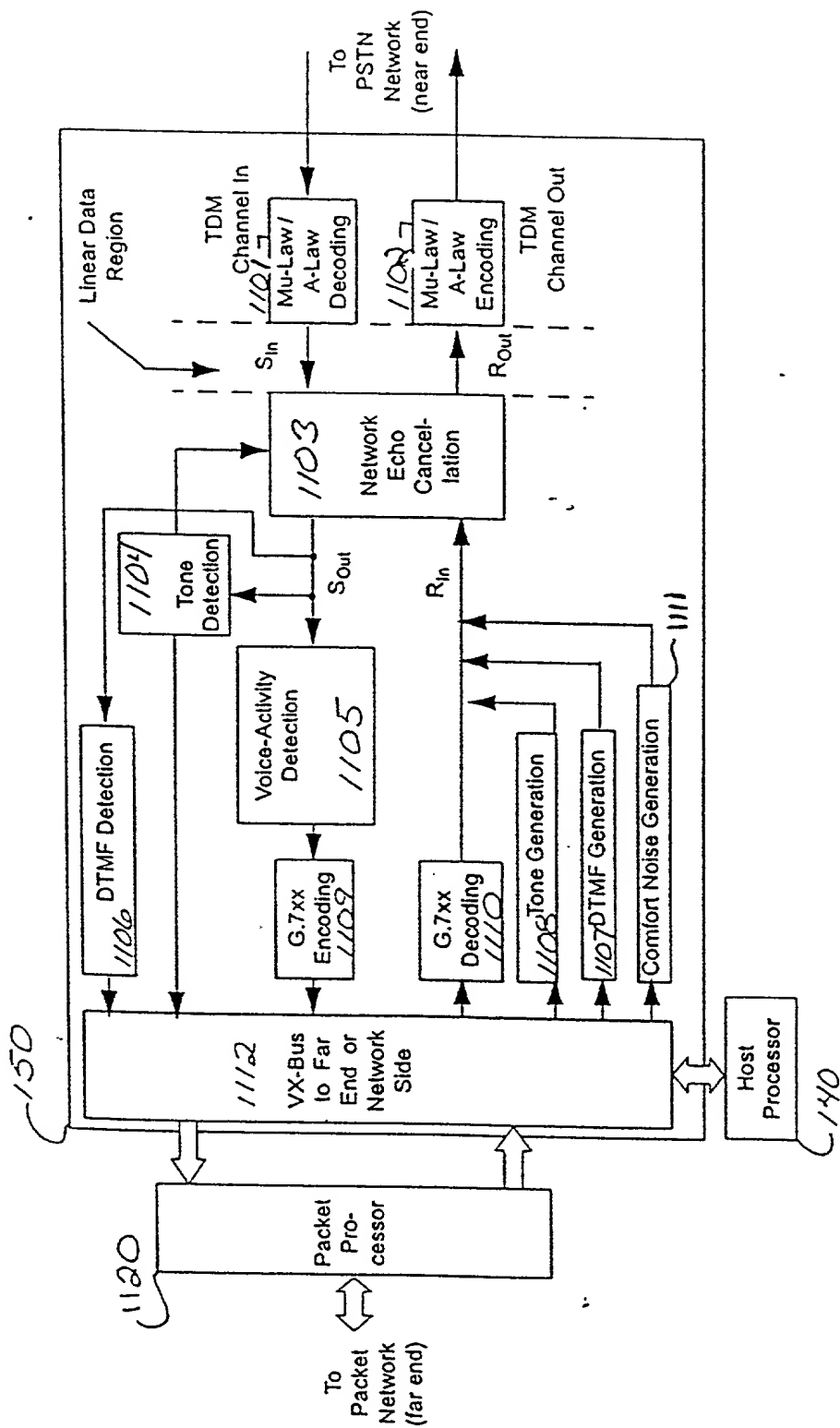
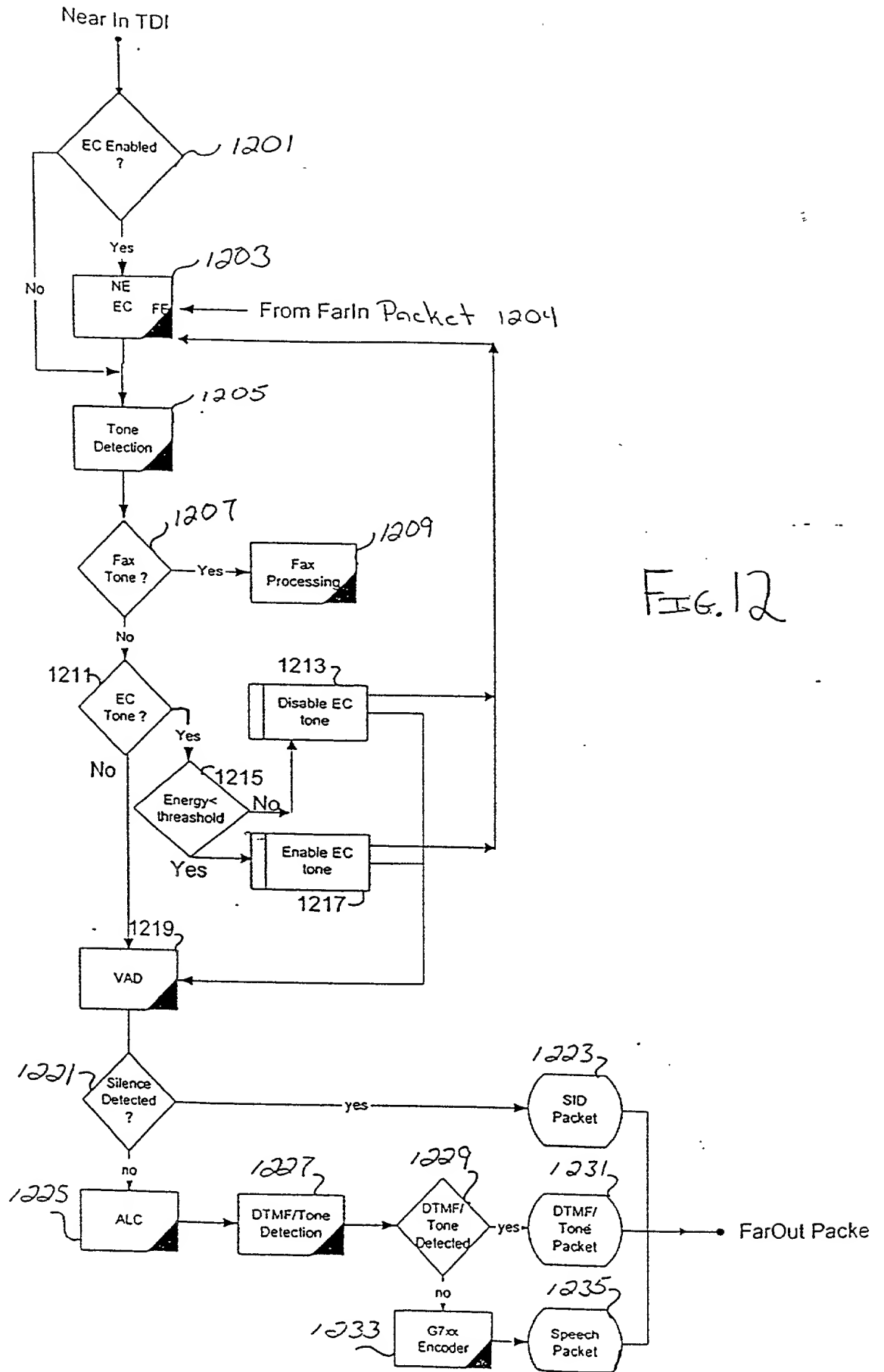


FIG. 11



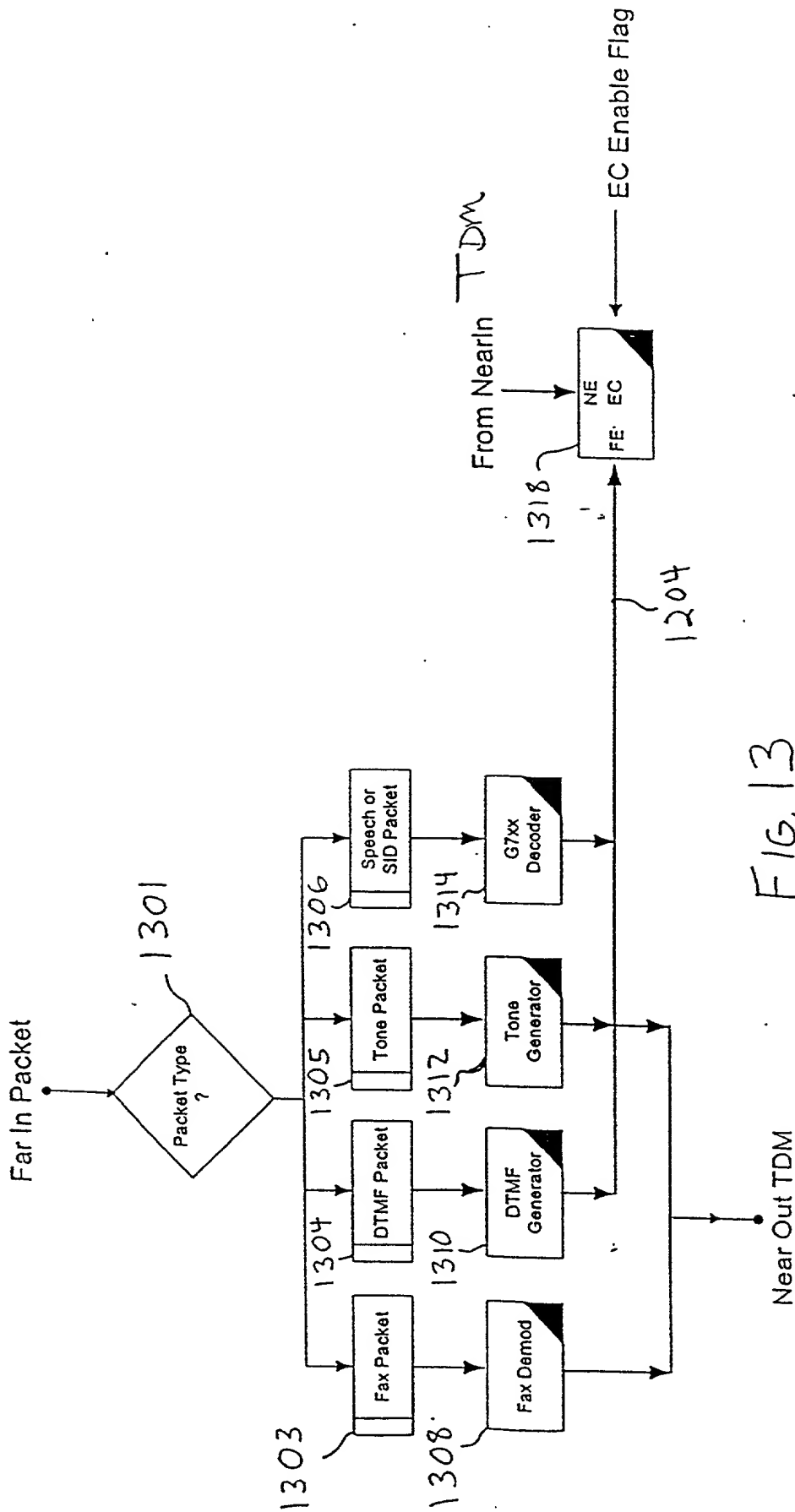


FIG. 13

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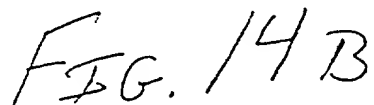


FIG. 14B

FFT Processing of Input Speech for VAD 1451

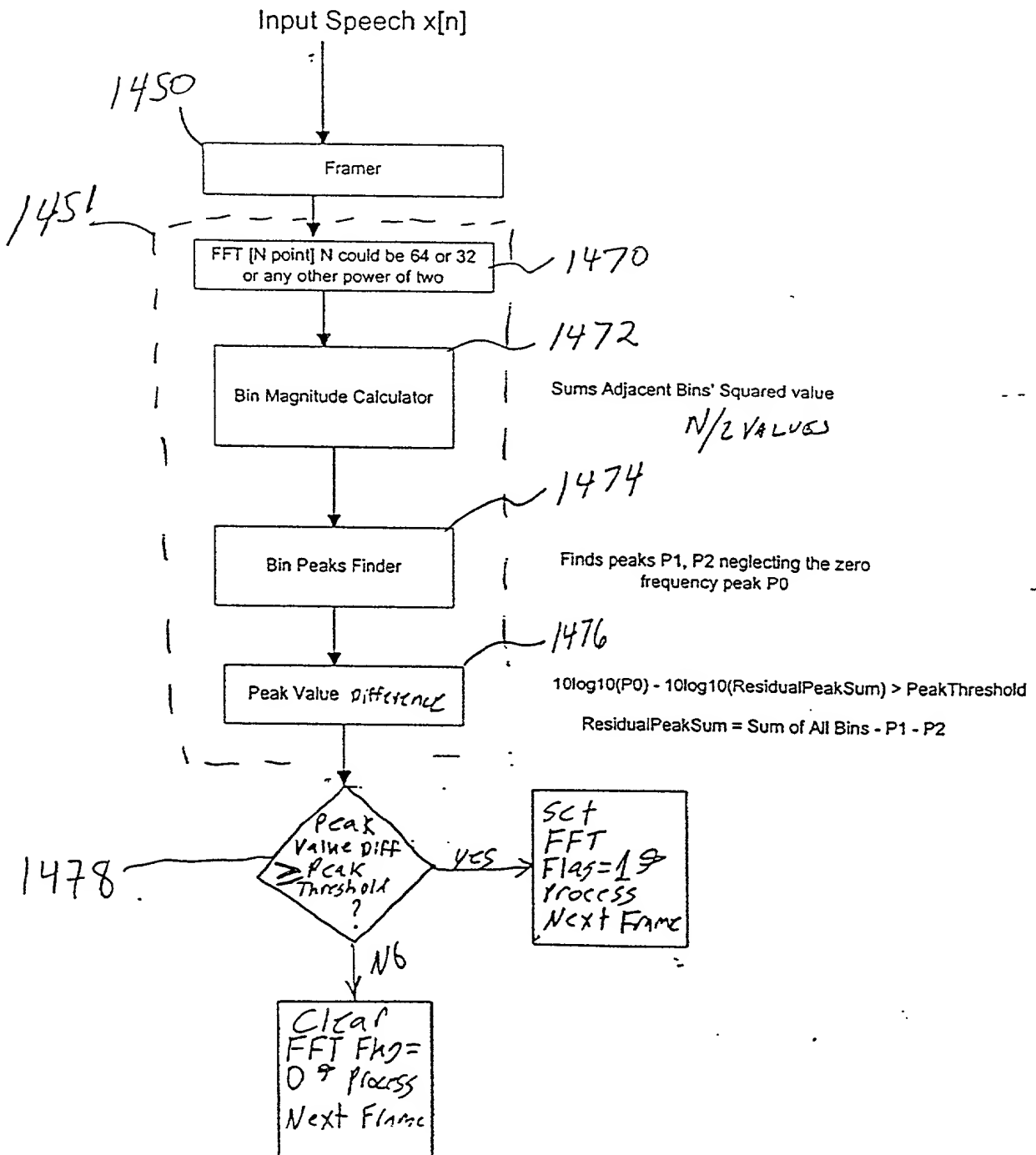


FIG. 14C

Zero Crossing Detector 1452

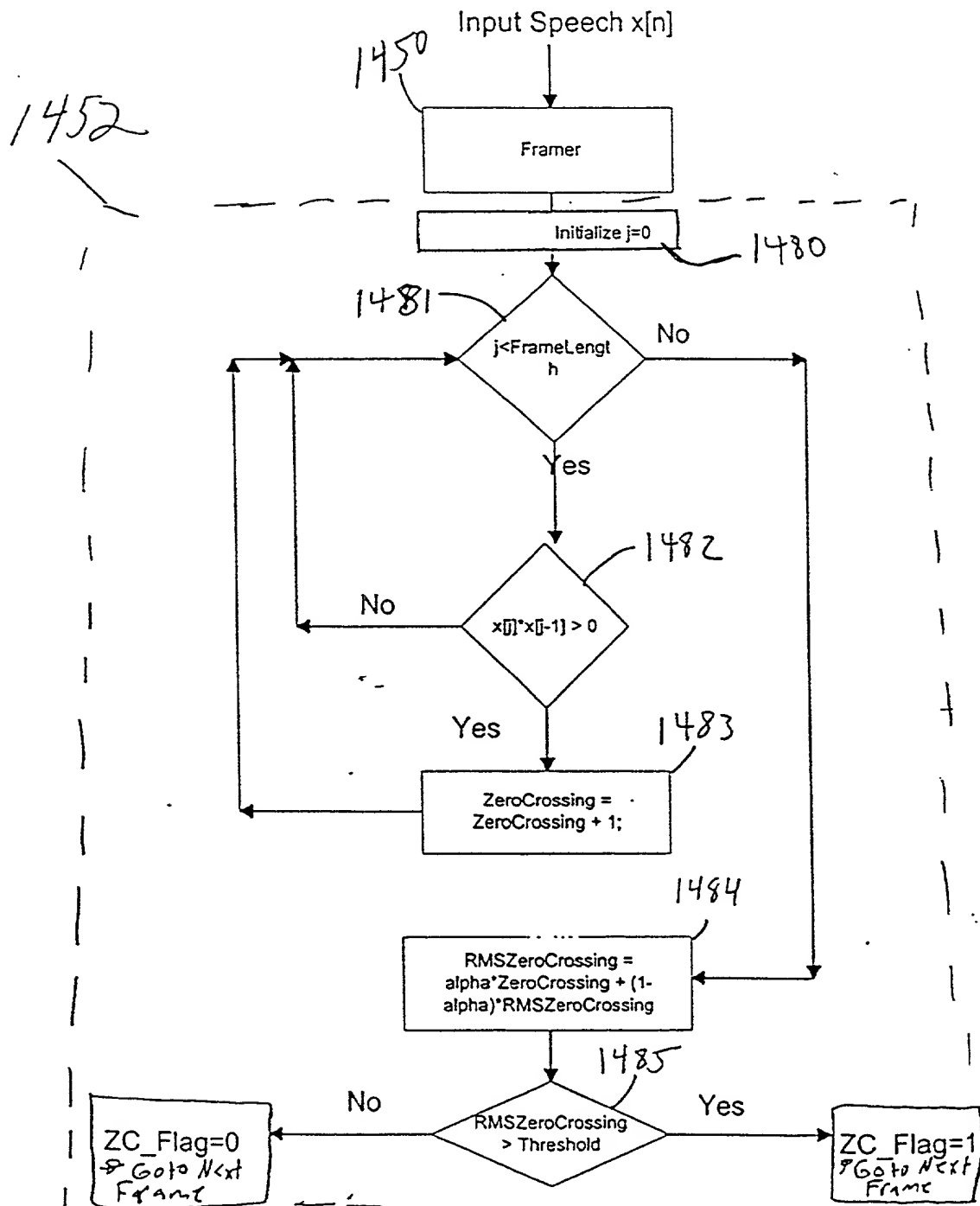


FIG. 14D

Noise Detection in VAD 145.

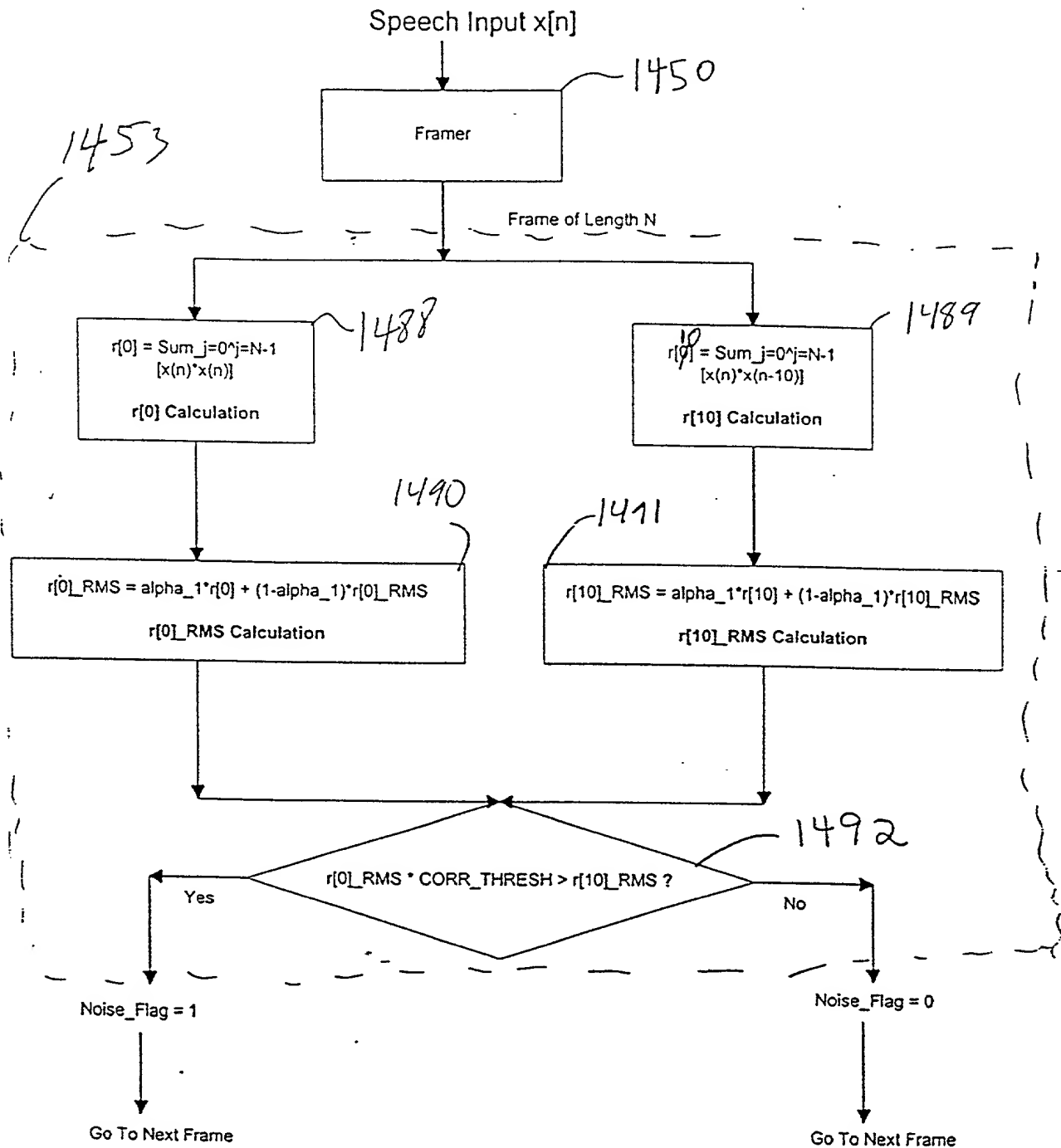


FIG. 14E

0933104-03601

Energy Discriminator 1454

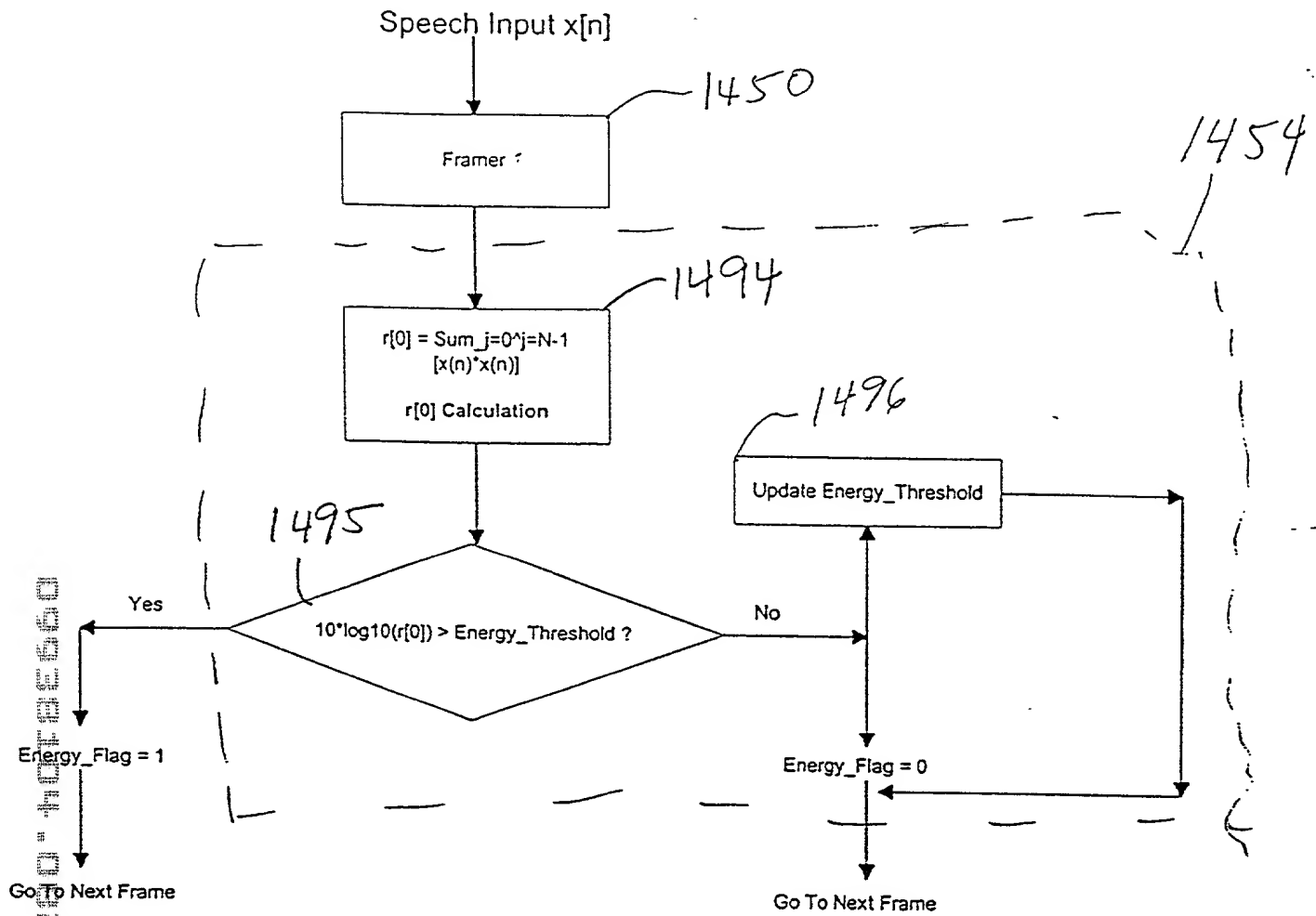


FIG. 14F

Instantaneous Energy Discriminator

1455

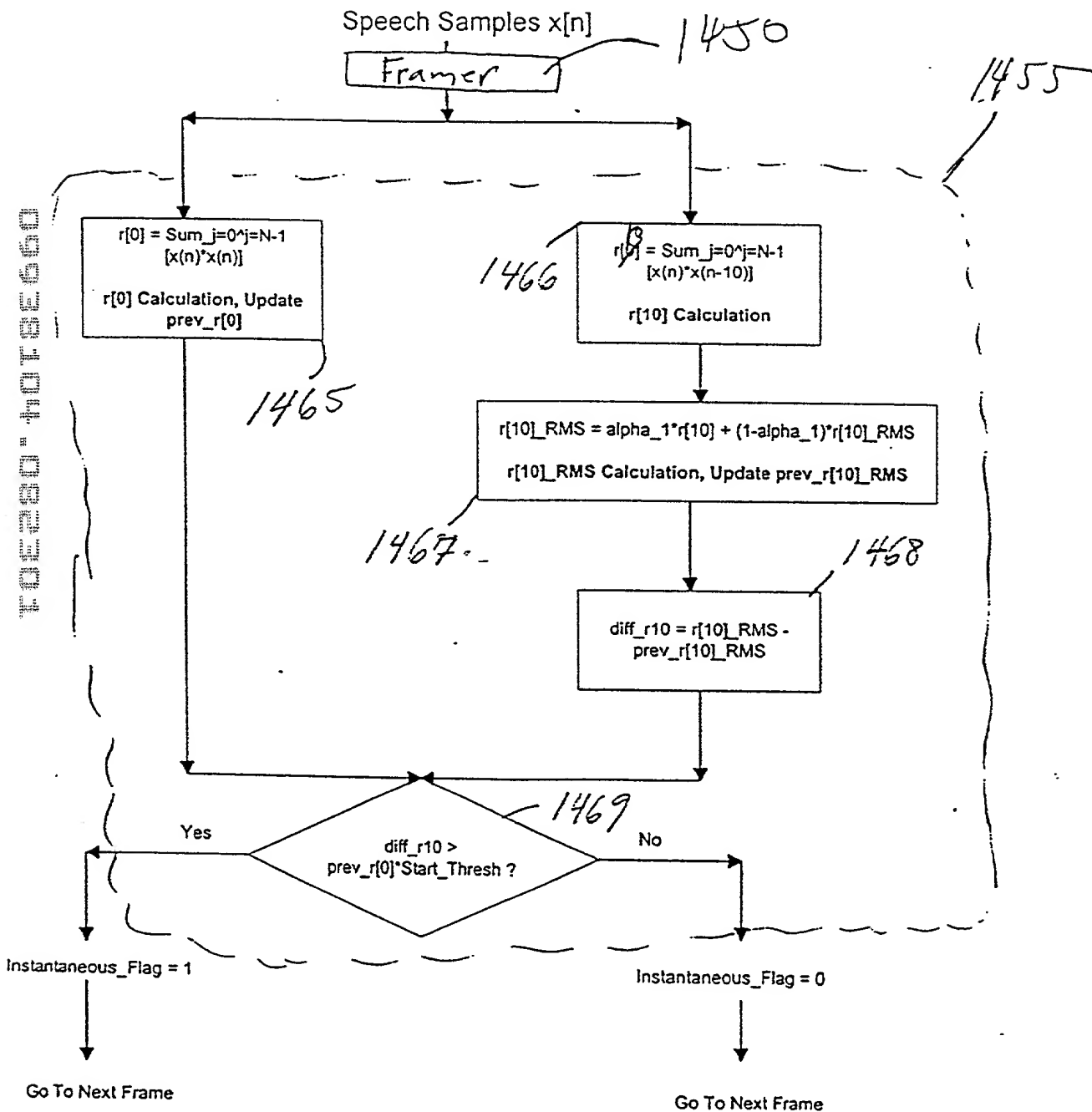


FIG. 14G

413

Core 2
Registers I/O Space

Core 2
Program and Data Memory

Core 1
Vector Area

Core 0
Script Code

Core 0
DTMF Code

Core 0
EC Code

Core 0
Reserved

Core 0
Kernel Reserved Location

Core 0
Script Data

Core 0
Inter Function Block Area

Core 0
DTMF Constants

Core 0
DTMF Parameters

Core 0
CHn DTMF Dynamic Data

Core 0
EC Constants

Core 0
EC Parameters

Core 0
CHn EC Dynamic Data

Core 0
CHn Near In Frame Data

Core 0
CHn Near Out Frame Data

Core 0
CHn Far In Frame Data

Core 0
CHn Far Out Frame Data

Core 0
Reserved

Core 0
Core 3

Core 0
Data

Core 0
Reserved

Core 0
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Fig. 15

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204A

202B
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204B

202C
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204C

202D
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204D

202E
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204E

202F
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204F

202G
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204G

202H
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204H

202I
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204I

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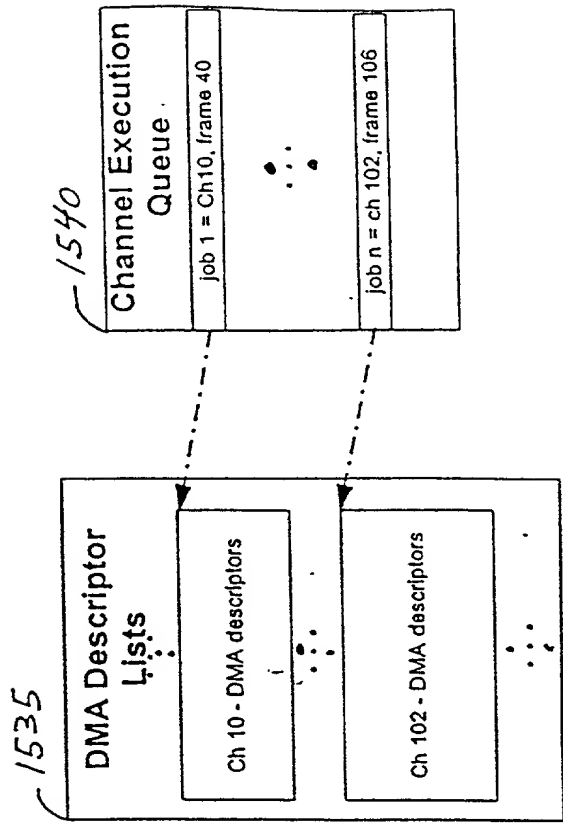
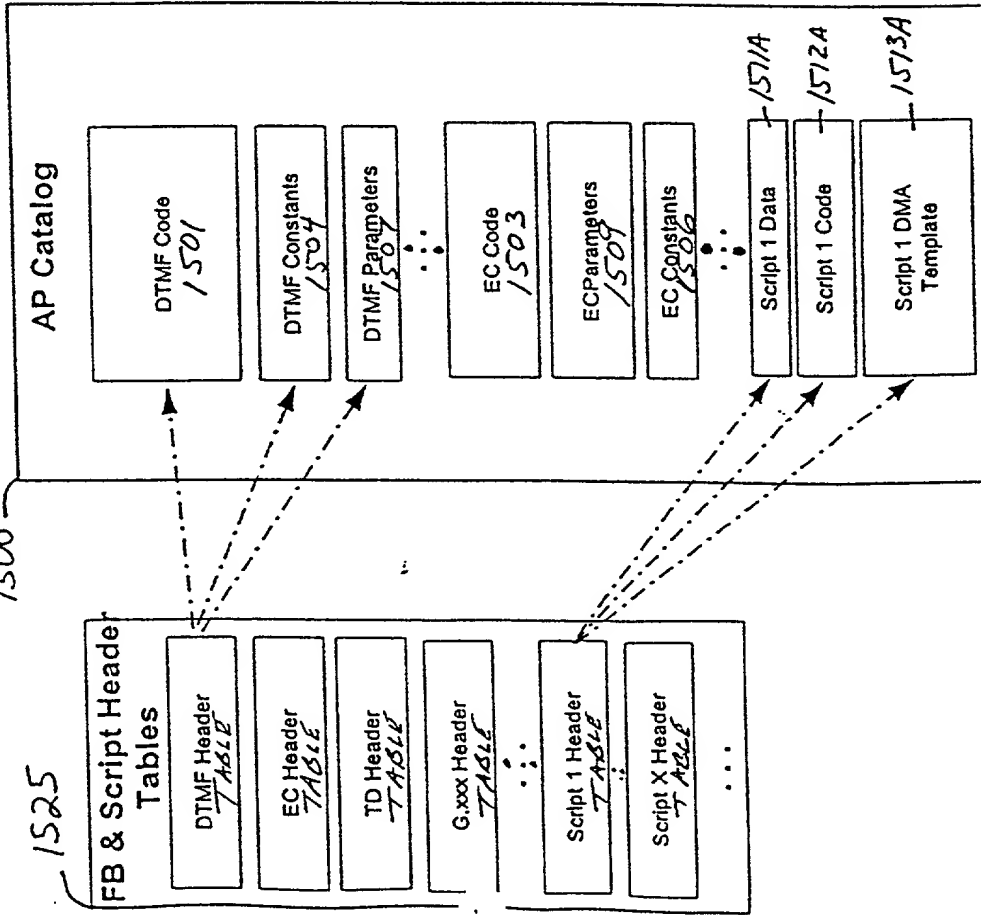
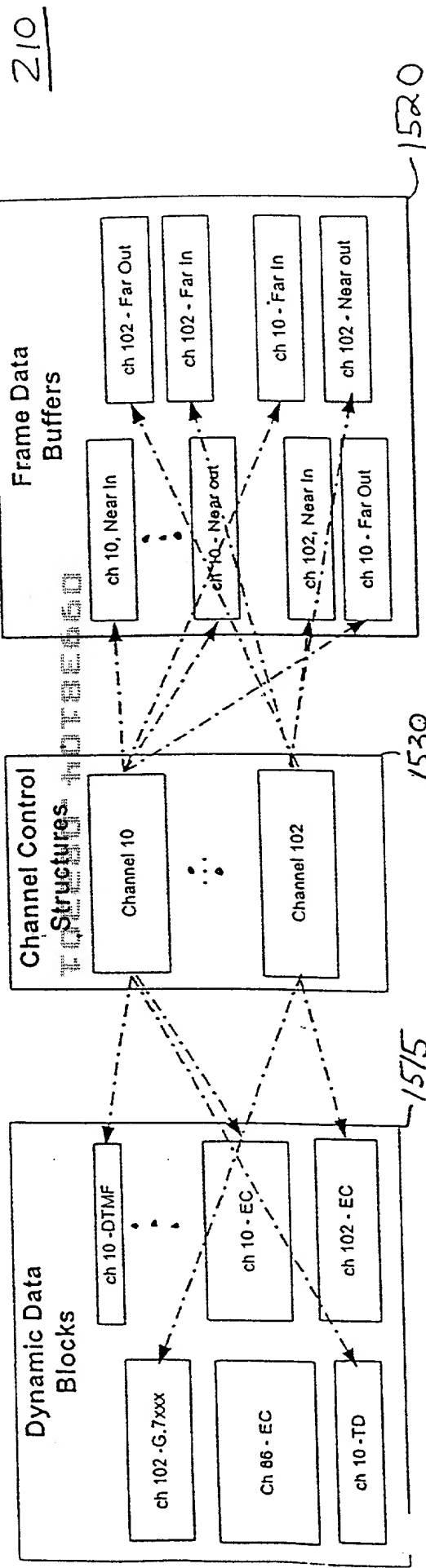


FIG 16

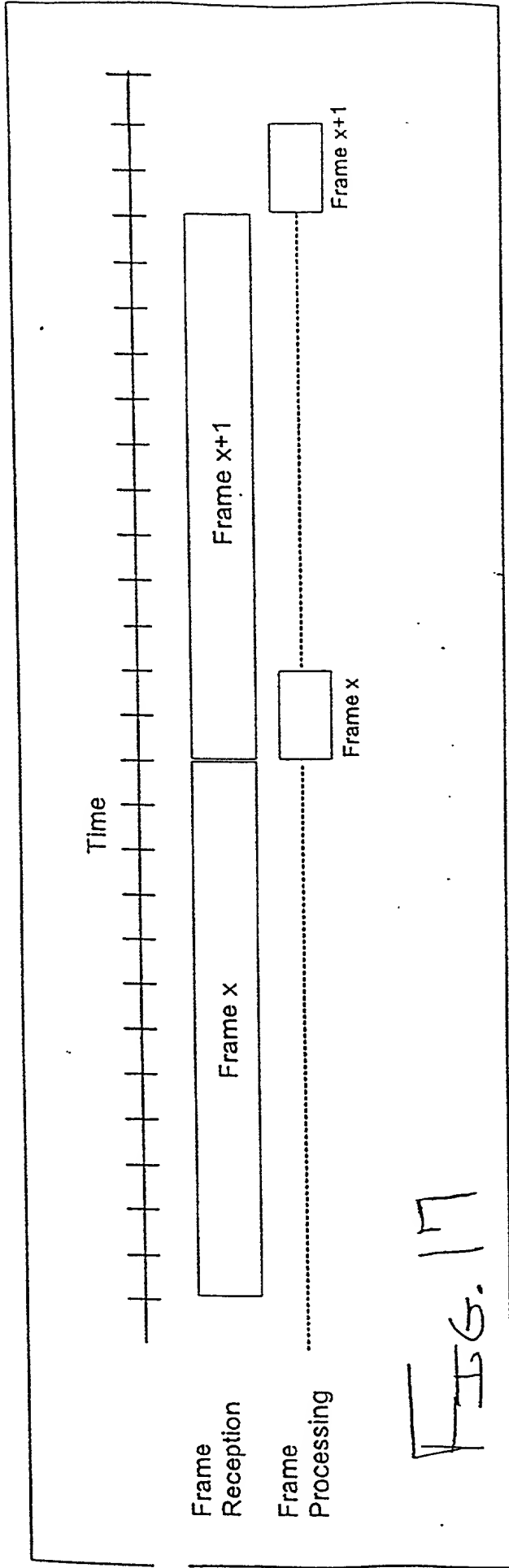


FIG. 17

FIG. 18

